IN THE CLAIMS

Please amend claim 14 as follows.

1. (Original) A display element drive circuit comprising an output stage including a CMOS circuit for driving a line to which a plurality of display elements are connected, wherein said CMOS circuit comprises a first P channel transistor and a second N channel transistor and a drive circuit for driving said first and second transistors, said drive circuit comprising a time constant circuit having a first time constant utilizing a first gate input capacitance of said first transistor and a second time constant utilizing a second gate input capacitance of said second transistor, one of the first and second time constants being selected such that, when said drive circuit receives a predetermined logic signal, one of said first and second transistors is turned ON after the other transistor is turned OFF.

2. (Original) A display element drive circuit as claimed in claim 1, wherein said drive circuit, when receives the predetermined logic signal, turns said first transistor ON after said second transistor is turned OFF, the first time constant is larger than the second time constant, the predetermined logic signal is either a High level or a Low level and said time constant circuit includes a first resistor coupled with said first gate input capacitance for determining

the first time constant and a second resistor coupled with said second gate input capacitance for determining the second time constant.

3. (Original) A display element drive circuit as claimed in claim 2, wherein the predetermined logic signal is the High level, the first time constant is a discharging time constant, which is 15 times the second time constant or more, said first and second resistors are connected in series with each other, at least said second resistor is an ON resistance of a third transistor, the first time constant is determined by the first gate input capacitance and a composite resistance value of said first resistor and the ON resistance of said third transistor, the second time constant is determined by the second gate input capacitance and the ON resistance of said third transistor and said time constant circuit operates when said third transistor is turned ON in response to the High level logic signal.

4. (Original) A display element drive circuit as claimed in claim 3, wherein said time constant circuit further has a third time constant utilizing the first gate input capacitance and a fourth time constant utilizing the second gate input capacitance and either the third or fourth time constant is selected such that said second transistor is

turned ON after said first transistor is turned OFF, when said drive circuit receives the other logic signal.

5. (Original) A display element drive circuit as claimed in claim 4, wherein the fourth time constant is larger than the third time constant and said time constant circuit includes a third resistor coupled with the first gate input capacitance for determining the third time constant and a fourth resistor coupled with the second gate input capacitance for determining the fourth time constant.

6. (Original) A display element drive circuit as claimed in claim 5, wherein the fourth time constant is a charging time constant, which is 15 times the third time constant or more, said third and fourth resistors are connected in series with each other, said third resistor is an ON resistance of a fourth transistor, said fourth resistor is an ON resistance of a fifth transistor, the third time constant is determined by the first gate input capacitance and the ON resistance of said fourth transistor, the fourth time constant is determined by the second gate input capacitance and a composite resistance value of the ON resistances of said fourth and fifth transistors and said time constant circuit operates when said fourth and fifth transistors are turned ON in response to the Low level logic signal.

7. (Original) A display element drive circuit as claimed in claim 6, wherein one end of said first resistor, which is connected to said third transistor, is connected to a gate of said second transistor, the other end of said first resistor is connected to a gate of said first transistor and said fourth transistor and said fifth transistor is provided in parallel to said first resistor.

8. (Original) A display element drive circuit as claimed in claim 7, wherein said third transistor is an N channel transistor, said fourth transistor is a P channel transistor, one end of said first resistor is grounded through said third transistor, the other end of said first resistor is connected to a power source line through said fourth transistor and said fifth transistor is turned ON in response to one of the High and Low levels and OFF in response to the other level.

9. (Original) A display element drive circuit as claimed in claim 2, wherein said display element is an organic EL element and a cathode side terminal of said organic EL is connected to said line.

10. (Original) A display element drive circuit as claimed in claim 5, wherein said drive circuit includes two P channel transistors having source-drain circuits connected in

series and an N channel transistor having a drain connected to the source of a downstream side one of said P channel transistors between a power source line and a ground, said first resistor is one of said P channel transistors, which is not connected to said power source line, said second resistor is an ON resistance of said N channel transistor, said third resistor is an ON resistance of the other of said P channel transistors and said fourth resistor is said one of said P channel transistors.

11. (Original) A display element drive circuit as claimed in claim 5, wherein said drive circuit includes a P channel transistor and two N channel transistors having drain-source circuits connected in series to a downstream side of said P channel transistor between a power source line and a ground, said first resistor is an ON resistance of one of said N channel transistors, which is connected to said P channel transistor, said second resistor is an ON resistance of the other of said N channel transistors, said third resistor is an ON resistance of said P channel transistor and said fourth resistor is provided in parallel to said first resistor.

12. (Original) A display element drive circuit as claimed in claim 1, wherein one of the first and second time constants is selected such that said second transistor is turned ON after said first transistor is turned OFF in

response to a predetermined logic signal inputted to said drive circuit, the first time constant is smaller than the second time constant, the predetermined logic signal is either a High level or a Low level and said time constant circuit includes a first resistor coupled with the first gate input capacitance for determining the first time constant and a second resistor coupled with the second gate input capacitance for determining the second time constant.

13. (Original) A display element drive circuit as claimed in claim 12, wherein the predetermined logic signal is Low level, the first time constant is a discharging time constant equal to one-fifteenth of the second time constant or smaller, said first and second resistors are connected in series with each other, at least said first resistor is an ON resistance of a third transistor, the first time constant is determined by the first gate input capacitance and the ON resistance of said third transistor, the second time constant is determined by the second gate input capacitance and a sum of the On resistance of said third transistor and said second resistor and said time constant circuit operates when said third transistor is turned ON in response to the Low level signal.

14. (Currently Amended) A display device including a display element drive circuit claimed in ~~any of~~ claim~~s~~ 1 ~~to 13~~.